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Colleen J. Dew

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit 2822

In re application of	:	July 25, 2002
Axel Brintzinger et al.	:	Examiner: Monica Lewis
Serial No. : 09/873,537	:	
Filed: June 4, 2001	:	IBM Corporation Dept. 18G/Bldg, 300-482
Title: DUAL DAMASCENE ANTI-FUSE WITH VIA BEFORE WIRE	:	2070 Route 52 Hopewell Junction, NY 12533-6531

Request for Reconsideration

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Commissioner for Patents and Trademarks
Washington, D.C. 20231

Sir:

The following request for reconsideration is submitted in response to the final office action dated May 21, 2002.

The invention centers on novel interconnect structures having an anti-fuse formed as a layer having openings that defines via locations. The structures of the invention advantageously incorporate anti-fuses at reduced manufacturing cost.

Chang (US 5807786) disclose an interconnect structure comprising an amorphous silicon anti-fuse (7) formed over a via hole (3) which hole is defined in dielectric layer (2). In the via hole (3), a further dielectric (6) is located about

the top of the via hole as a part of a liner. Chang does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

Applicants note that the final office action calls layer 2 of Chang an antifuse dielectric layer. Applicants submit that this interpretation is incorrect and ignores the teaching of Chang as well as the commonly understood in the art. Chang specifically references layers 7 and 8 as representing a composite antifuse structure. See col. 3, lines 48+. Chang does not indicate layer 2 as being an antifuse layer. Layer 2 could never act as an antifuse in as much as the path formed by the real antifuse (7, 8) of Chang through the via (4, 5b) would always conduct electricity first, thus preventing accumulation of a sufficient voltage differential across diectric layer 2 for dielectric layer 2 to breakdown and act as a conductive pathway (i.e., for layer 2 to behave like an antifuse). Moreover, if layer 2 were an antifuse layer, the entire structure of Chang would short-circuit and be rendered inoperative since layer 2 is intended to be an insulator under all conditions of the interconnect/chip operation. Applicants submit that an interpretation of the reference which renders the device of the reference inoperative cannot be a proper basis for rejection of the claims under 35 USC 103.

Go et al. (US 5592016) discloses anti-fuse structures which are located above or below vias. Go et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

McCollum et al. (US 5770885) discloses a silicon oxynitride layer on a substrate over which an amorphous silicon anti-fuse is formed. McCollum et al. does not disclose or suggest an anti-fuse layer with an opening which defines a via location.

For the above reasons, applicants submit that the present claims are patentable over the prior art of record and that the application is in condition for allowance. Such allowance is earnestly and respectfully solicited.

Respectfully submitted,
Axel Brintzinger et al.

By _____
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CERTIFICATE OF TRANSMISSION BY FACSIMILE (37 CFR 1.8) Applicant(s): Axel Brintzinger et al.			Docket No. FIS920000011US2
Serial No. 09/873,537	Filing Date 06/04/2001	Examiner Monica Lewis	Group Art Unit 2822

Invention:

DUAL DAMASCENE ANTI-FUSE WITH VIA BEFORE WIRE

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